In the Claims

1. (currently amended) A semiconductor device comprising:

a semiconductor substrate assembly comprising:

a semiconductor wafer;

at least first and second doped areas in the wafer;

a first contact pad electrically coupled to the first doped area and a second contact pad electrically coupled to the second doped area;

a digit line contact plug portion comprising a lower surface and an upper surface wherein the upper surface is further away from the semiconductor substrate than the lower surface, and the lower surface contacts the first contact pad; ~~and~~

a capacitor storage node comprising a lower surface and an upper surface wherein the upper surface of the storage node is further away from the semiconductor substrate than the lower surface of the storage node and is at least as far away from the semiconductor substrate as the upper surface of the digit line contact plug portion; and

a dielectric layer interposed between the digit line contact plug portion and the capacitor storage node, and which contacts both the digit line contact plug portion and the capacitor storage node.

2. (original) The semiconductor device of claim 1 wherein the lower portion of the storage node is closer to the semiconductor substrate than the upper surface of the digit line contact plug portion.

3. (currently amended) The semiconductor device of claim ~~18~~ 1 wherein the digit line contact plug portion is a first portion, and the semiconductor device further comprises:

a second digit line contact plug portion having a lower surface which contacts the upper surface of the first portion of the digit line contact plug;

a capacitor top plate overlying the capacitor storage node; and

a dielectric spacer which contacts the top plate and which contacts the second digit line contact portion.

4. (original) The device of claim 3 further comprising:

a capacitor dielectric layer interposed between the capacitor storage node and the capacitor top plate;

a planarized dielectric layer overlying the capacitor top plate; and

the spacer having a first portion which is recessed within an opening defined by the planarized dielectric layer and the capacitor dielectric layer and further having a second portion which is not recessed within the opening,

wherein the first portion of the spacer overlies the capacitor dielectric layer and the second portion of the spacer does not overlie the capacitor dielectric layer.

5. (original) The semiconductor device of claim 3 wherein the second digit line contact plug portion comprises a conductive runner which overlies the capacitor storage node.

6. (currently amended) A semiconductor device comprising:

first and second spaced capacitor storage plates each having a generally horizontally-oriented lower surface, a generally horizontally-oriented upper surface, and a generally vertically-oriented surface interposed between the lower surface and the upper surface; ~~and~~

a contact plug having a generally horizontally-oriented lower surface and a generally horizontally-oriented upper surface,

wherein the contact plug is generally enclosed in an area which is defined, in cross section, by an upper boundary which extends from the upper surface of the first capacitor storage plate to the upper surface of the second capacitor storage plate, by a lower boundary which extends from the lower surface of the first capacitor storage plate to the lower surface of the second capacitor storage plate, and by a lateral boundary which is defined by the generally vertically-oriented surfaces of the first and second spaced capacitor storage plates; and

a dielectric layer interposed between the contact plug and each of the first and second spaced capacitor storage plates, wherein the dielectric layer contacts each of the first and second spaced capacitor storage plates and the contact plug.

7. (original) The device of claim 6 wherein the contact plug is a first contact plug and the semiconductor device further comprises:

a first capacitor top plate paired with the first capacitor storage plate and a second capacitor top plate paired with the second capacitor storage plate; and

a second contact plug having a lower surface which contacts the upper surface of the first contact plug and is interposed between the first and second capacitor top plates.

8. (original) The device of claim 7 wherein the second contact plug further comprises an upper portion which provides a conductive runner, the conductive runner overlying the first and second capacitor storage plates.

9. (original) The device of claim 7 further comprising:

a semiconductor wafer having first, second, and third conductively doped regions therein;

a first conductive contact pad electrically coupled with the first conductively doped region in the wafer, the lower surface of the first capacitor storage plate contacting the first conductive contact pad;

a second conductive contact pad electrically coupled with the second conductively doped region in the wafer, the lower surface of the first contact plug contacting the second conductive contact pad; and

a third conductive contact pad electrically coupled with the third conductively doped region in the wafer, the lower surface of the second capacitor storage plate contacting the third conductive contact pad.

10. (original) The device of claim 6 wherein the contact plug is a first contact plug and the semiconductor device further comprises:

a second contact plug having a lower surface which contacts the upper surface of the first contact plug and is interposed between the upper surface of the first capacitor storage plate and the upper surface of the second capacitor storage plate.

11. (currently amended) A semiconductor device comprising:

a semiconductor wafer having a conductively-doped region therein;

a first dielectric layer overlying the semiconductor wafer;

a conductive contact pad formed within the first dielectric layer and electrically coupled with the conductively-doped region of the semiconductor wafer;

a second dielectric layer;

a first portion of a digit line contact plug within and contacting the second dielectric layer and electrically coupled with the contact pad;

a capacitor storage node within and contacting the second dielectric layer;

a capacitor top plate layer having a portion overlying the storage node and overlying the first portion of the digit line contact plug, and further having an opening therein; and

a second portion of the digit line contact plug within the opening in the capacitor top plate layer.

12. (original) The semiconductor device of claim 11 further comprising:

first and second cross-sectional sidewalls in the top plate layer; and

first and second cross-sectional spacers which electrically insulate the capacitor top plate layer from the second portion of the digit line contact plug.

13. (new) The semiconductor device of claim 1 wherein a majority of a thickness of the dielectric layer is interposed between the digit line contact plug portion and the capacitor storage node.

14. (new) The semiconductor device of claim 6 wherein a majority of a thickness of the dielectric layer is interposed between the contact plug and each of the first and second spaced capacitor storage plates.

15. (new) The semiconductor device of claim 11 wherein a majority of a thickness of the second dielectric layer is interposed between the first portion of the digit line contact plug and the capacitor storage node.

16. (new) A semiconductor device comprising:

a semiconductor substrate assembly comprising a first contact pad and a second contact pad;

a digit line contact plug portion comprising a lower surface and an upper surface wherein the upper surface is further away from the semiconductor substrate than the lower surface, and digit line contact plug portion is electrically coupled with the first contact pad;

a capacitor storage node comprising a lower surface and an upper surface wherein the upper surface of the storage node is further away from the semiconductor substrate than the lower surface of the storage node and is at least as far away from the semiconductor substrate as the upper surface of the digit line contact plug portion;

a capacitor dielectric layer overlying the capacitor storage node;

a capacitor top plate overlying the capacitor storage node;

a dielectric layer overlying the capacitor top plate; and

a spacer having a first portion which contacts the capacitor top plate and which is recessed within an opening defined by the dielectric layer and the capacitor dielectric layer and further having a second portion which is not recessed within the opening.

17. (new) The semiconductor device of claim 16 wherein the dielectric layer overlying the capacitor top plate is a first dielectric layer and the semiconductor device further comprises a second dielectric layer interposed between the digit line contact plug portion and the capacitor storage node, wherein the second dielectric layer contacts both the digit line contact plug portion and the capacitor storage node.

18. (new) The semiconductor device of claim 17 wherein a majority of a thickness of the second dielectric layer is interposed between the digit line contact plug portion and the capacitor storage node.